## DETAILED ACTION

### *Specification*

The disclosure is objected to because of the following informalities:

improper grammar: Paragraph 0005, "the protect technologies in microcomputer with built-in…"; Page 10, "for supplementary illustrating a memory map"; Paragraph 0021 "described in detail base on the drawings";

unclear language: Paragraph 0011, "summary of a representative one of invention"; Paragraph 0018, "the representative one of invention"; the examiner suggests using the word "embodiment" instead of "one";

unmatched parenthesis, Paragraph 0059.

Appropriate correction is required.

### *Claim Objections*

Claim 9 is objected to because of the following informalities: improper grammar: "an rewrite". Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 8, the phrase "in the case where erasure operation of the memory array unit occurs" would indicate to one of ordinary skill in the art that an actual erasure has taken place, but the erasure control circuit may prohibit such an erasure. The entire phrase has been construed as "in the case where an erasure instruction is received by the memory array unit."

Regarding Claim 10, the phrase "when rewrite operation of the memory array unit occurs" would indicate to one of ordinary skill in the art that an actual rewrite has taken place, but the rewrite control circuit may prohibit such a rewrite. The entire phrase has been construed as "when a rewrite instruction is received by the memory array unit."

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Coulier at al (US 5,963,980).

Regarding Claim 1, Coulier teaches a semiconductor integrated circuit apparatus comprising:

a nonvolatile storage provided with a memory array unit (Column 3 Line 32) having a plurality of nonvolatile memory cells (memory is inherently composed of cells to store data) and a control unit for controlling write operation of storing information in

the nonvolatile memory cells, read operation of reading out the information stored in the nonvolatile memory cells, and erase operation of erasing the information stored in the nonvolatile memory cells (such a control unit must be present to modify the nonvolatile memory as described by Coulier on Column 2 Lines 3-4 and for loading and unloading programs from the memory as described on Column 5 Lines 36-40, also note that the "user memory" is used by Coulier to mean the non-volatile memory, see Column 2 Lines 1-5);

a volatile storage (RAM MT, see Figure 2) to be used as a work area of a program stored in the nonvolatile storage (see Figure 2 and how the programs in the non-volatile memory have a corresponding program section in the RAM, also see the general description of this working memory on Column 1 Lines 31-35);

a central processing unit capable of executing a predetermined processing and giving instructions to the nonvolatile storage (Column 3 Lines 34-36, also see the commands a CPU may give to a memory on Column 1 Lines 49-56);

a protect operation control unit for controlling the nonvolatile storage and the read operation of the nonvolatile storage (Column 4 Lines 52-59), wherein the memory array unit has a first protect memory area in which reading and writing of information stored are prohibited under the control of the protect operation control unit (note in Figure 2 how each application has its own zone, which is a protected memory area, see Column 4 Lines 63-65, also see the possible restrictions given to the protected memory areas shown on Figure 3 on Column 5 Line 62 to Column 6 Line 18);

the volatile storage has a second protect memory area (see Figure 2 and how the RAM is partitioned into protected memory areas) in which reading from an area other than the first protect memory area of the memory array unit is prohibited under the control of the protect operation control unit (see Figures 3, also see the possible restrictions given to these areas on Column 5 Line 62 to Column 6 Line 18); and

the second protect memory area of the volatile storage is used as a work area of a program stored in the first protect memory area of the nonvolatile storage (see Figure 2 and how the programs in the non-volatile memory have a corresponding program section in the RAM, also see the general description of this working memory on Column 1 Lines 31-35).

Regarding Claim 2, Coulier teaches a semiconductor integrated circuit apparatus comprising:

a nonvolatile storage provided with a memory array unit (Column 3 Line 32) having a plurality of nonvolatile memory cells (memory is inherently composed of cells to store data) and a control unit for controlling write operation of storing information in the nonvolatile memory cells, read operation of reading out the information stored in the nonvolatile memory cells, and erase operation of erasing the information stored in the nonvolatile memory cells (such a control unit must be present to modify the nonvolatile memory as described by Coulier on Column 2 Lines 3-4 and for loading and unloading programs from the memory on Column 5 Lines 36-40, also note that the “user memory” is used by Coulier to mean the non-volatile memory, see Column 2 Lines 1-5);

a volatile storage (RAM MT, see Figure 2);

a central processing unit capable of executing a predetermined processing and giving instructions to the nonvolatile storage (Column 3 Lines 34-36, also see the commands a CPU may give to a memory on Column 1 Lines 49-56); and

a protect operation control unit for controlling the nonvolatile storage and the read operation of the nonvolatile storage (Column 4 Lines 52-59), wherein the memory array unit has a first protect memory area in which reading and writing of information stored are prohibited under the control of the protect operation control unit (note how each application has its own zone, which is a protected memory area, see Column 4 Lines 63-65, also see the possible restrictions given to these areas on Column 6 Lines 19-43); and

the volatile storage has a second protect memory area (see Figure 2 and how the RAM is partitioned into protected memory areas) in which reading from an area other than the first protect memory area of the memory array unit is prohibited under the control of the protect operation control unit (see Figures 3, also see the possible restrictions given to these areas on Column 5 Line 62 to Column 6 Line 18).

Claim 11 is the electric system corresponding to the integrated circuit of Claim 1 and is rejected on the same grounds.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-6, 12-13, and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coulier in view of Guttag et al (US 4,590,552).

Regarding Claim 3, Coulier teaches all limitations of Claim 1 as discussed above. However, while Coulier mentions comparing addresses (see the means for comparing of Coulier's Claim 1), he does not say if the memory access instruction is compared to limits where the instruction could be inside the first protect memory area. Guttag teaches a comparison circuit that judges whether or not an address signal from the central processing unit is inside a protected memory area (Column 4 Lines 27-31 in Guttag). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used such comparison logic in the device described by Coulier because the protected ranges can be easily expanded or contracted using the address registers. Guttag implies this by stating the versatility of such a method (Column 4 Line 27 in Guttag).

This combined device meets all limitations of Claim 4, since it meets all limitations of Claim 3 as described above, wherein the protect operation control unit compares an address signal output from the central processing unit with a value of a program counter (Column 4 Lines 27-31 in Guttag, note how the address bus corresponds to the address signal from the central processing unit and the range of addresses in a protected memory area, or the program, corresponds to a value from the program counter) to permit reading in the first protect memory area only in the case where the address signal and the program counter value are address values inside the

first protect memory area (see Column 4 Lines 5-13 in Coulier, where an access check is performed for each instruction and clearance must be given, also see Column 4 Lines 55-56 where it is more specifically stated that access must be given to read information).

Since Claims 5 and 6 are equivalent to Claims 3 and 4 except that Claims 5 and 6 are directed to protecting volatile memory (in the second protect area) instead of nonvolatile memory (in the first protect area). Since Guttag's circuitry applies to both RAM and nonvolatile memory devices (see Column 4 Lines 10-12 in Guttag), Claims 5 and 6 are rejected on the same grounds as Claims 3 and 4.

Regarding Claim 12, Coulier teaches all limitations of Claim 11 as described above. However, while Coulier mentions comparing addresses (see the means for comparing of Claim 1), he does not say if the memory access instruction is compared to limits where the instruction could be inside the first or second protect memory area. Guttag teaches a comparison circuit that judges whether or not an address signal from the central processing unit is inside a protected memory area (Column 4 Lines 27-31 in Guttag). Note that this can apply to RAM (as in the second protect memory area, see Column 4 Lines 10-12 in Guttag) and nonvolatile memory (as in the first protect memory area). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used such comparison logic in the device described by Coulier because the protected ranges can be easily expanded or contracted using the address registers. Guttag implies this by stating the versatility of such a method (Column 4 Line 27 in Guttag).

Regarding Claim 13, the combined device meets all limitations of Claim 12, and the further limitations are the same as those of Claim 4, and thus Claim 13 is rejected on the same grounds as the previous Claims.

Regarding Claim 16, since Coulier meets all limitations of Claim 2, Claim 2 is broader than Claim 1, and the only further limitation is the same as that of Claim 3, Claim 16 is rejected on the same grounds as those previous claims.

Regarding Claim 17, since the combined device meets all limitations of Claim 16 and the only further limitation is the same as that of Claim 4, Claim 17 is rejected on the same grounds as those previous claims.

Regarding Claim 18, since Coulier meets all limitations of Claim 2, Claim 2 is broader than Claim 1, and the only further limitation is that of Claim 5, Claim 18 is rejected on the same grounds as those previous claims.

Regarding Claim 19, since the combined device meets all limitations of Claim 18 and the only further limitation is the same as that of Claim 6, Claim 19 is rejected on the same grounds as those previous claims.

Claims 7, 9, 14-15, 20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coulier in view of Fukumoto et al (US 5,673,222).

Regarding Claim 7, Coulier teaches all limitations of Claim 1 as discussed above. However, Coulier does not teach an erasure prohibition control unit for prohibiting erasure in the first protect memory area. Fukumoto teaches an erasure prohibition control unit to prevent certain blocks of the memory from being written to (see the Write

Protect Signal Generator of Figure 5 in Fukumoto, also see description of how the Write Protect signal operates on Column 16 Lines 1-10, Column 16 Lines 54-65, and Figure 4 in Fukumoto). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used this circuit described by Fukumoto to prohibit erasure in the first protect memory area because it stops important data stored in the chip from being erased by mistake (see Column 5 Lines 8-10 in Fukumoto).

This combined device meets all limitations of Claim 9, since Coulier teaches all limitations of Claim 1 as described above, further comprising a rewrite prohibition control unit for prohibiting rewrite in the first protect memory area (note that the erasure prohibition control unit described by Fukumoto also acts to prohibit writes and writing to a memory location with data is a rewrite, see Column 16 Lines 1-6 in Fukumoto).

Claims 14 and 15 are the corresponding electrical system claims to the circuit of Claims 7 and 9, respectively. Thus, they are rejected on the same grounds.

Regarding Claim 20, since Claim 2 is broader than Claim 1 and the only further limitation is the same as that of Claim 7, it is rejected on the same grounds as those previous claims.

Regarding Claim 22, since Claim 2 is broader than Claim 1 and the only further limitation is the same as that of Claim 9, it is rejected on the same grounds as those previous claims.

Claims 8 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coulier and Fukumoto as applied to claims 7 and 9 above, and further in view of Pritchard et al (US 2002/0166067) and Jones et al (5,623,637).

Regarding Claim 8, Coulier and Fukumoto meet all limitations of Claim 7 as described above, wherein the erasure prohibition control unit is provided with a key code generation circuit for outputting a previously set key code signal (see comparators 15 and 20 in Figure 5, note how each comparator has as an input a previously set key code signal, also see Column 16 Line 54-65 in Fukumoto).

Though Fukumoto teaches this key code signal being compared with a different key code (Column 16 Lines 54-58, note the comparison between the previously described key code and a separate key code on the address and data lines), Fukumoto is silent on where this second key is stored. Jones teaches storing a password (or key) in an EEPROM to bar unauthorized access to information (Column 8 Lines 52-58, also see Password 301 on Figure 2 in Jones). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have stored the key described by Fukumoto in a nonvolatile memory such as that described by Jones since, if the key is always stored with the application it secures, it is guaranteed that you will always be able to secure the application when the proper circuitry is present.

Also, though Fukumoto teaches that when the keys coincide to grant permission to perform operations on the memory (see operation of WP signal on Figure 4), he does not teach prohibiting erasure in such a case. Pritchard teaches prohibiting erasure if

there is no intrusion (i.e., the key codes coincide, see steps 340 and 390 in Figure 3 in Pritchard, also note that the mass storage could be nonvolatile memory, see paragraph 0031 in Pritchard). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have provided such functionality in the erasure prohibition control unit for all instructions to the nonvolatile memory (including an erasure operation) described by Fukumoto since the device is then protected against viruses for all commands and allows for a clean reinstallation of the operating system (see Paragraph 0009 in Pritchard).

Regarding Claim 21, since the combined device of Coulier and Fukumoto teaches all limitations of Claim 20 and the only further limitation is the same as that of Claim 8, it is rejected on the same grounds as those previous claims.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coulier, Fukumoto, Pritchard, and Jones, and further in view of Guttag (4,590,552). Coulier and Fukumoto teach all limitations of Claim 9 as described above, wherein the rewrite prohibition control unit is provided with:

a key code generation circuit for outputting a previously set key code signal (see comparators 15 and 20 in Figure 5, note how each comparator has as an input a previously set key code signal, also see Column 16 Line 54-65 in Fukumoto); and

a key code judgment unit for comparing a key code signal generated by the key code generation circuit and a key code stored in the first protect memory area and outputting a coincidence signal when the key codes coincide with each other

(analogous to the key code comparison technique described in Claim 8 from the teachings of Fukumoto and Jones).

However, while Coulier mentions comparing addresses (see the means for comparing of Claim 1), there is no address judgment unit for judging whether or not the rewrite destination address signal is in the first protect memory area. Guttag teaches a comparison circuit that judges whether or not an address signal from the central processing unit is inside a protected memory area (Column 4 Lines 27-31 in Guttag). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used such comparison logic in the device described by Coulier because the protected ranges can be easily expanded or contracted using the address registers. Guttag implies this by stating the versatility of such a method (Column 4 Line 27 in Guttag).

Also, though Fukumoto teaches that when the keys coincide to grant permission to perform operations on the memory (see operation of WP signal on Figure 4), he does not teach prohibiting a rewrite in such a case. Pritchard teaches prohibiting a rewrite of the operating system if there is no intrusion (i.e., the key codes coincide, see steps 340 and 390 in Figure 3 in Pritchard, also note that the mass storage could be nonvolatile memory, see paragraph 0031 in Pritchard) and the destination address is in the first protect memory area (the part of the mass storage device containing the operating system is considered the first protect memory area, note how the operating system is rewritten on paragraphs 0047 and 0048 in Pritchard). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject

matter pertains to have provided such functionality for all instructions to the nonvolatile memory (including the rewrite instruction) in the rewrite prohibition control unit described by Fukumoto since the device is then protected against viruses and allows for a clean reinstallation of the operating system (see Paragraph 0009 in Pritchard).

Regarding Claim 23, since the combined device of Coulier and Fukumoto teaches all limitations of Claim 21 and the only further limitation is the same as that of Claim 10, it is rejected on the same grounds as those previous claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark A. Giardino whose telephone number is (571) 270-3565. The examiner can normally be reached on M-R 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Robertson can be reached on (571) 272-4186. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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